CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of forming a MOSFET device comprising the steps of:

providing a structure comprising a dummy gate that has an upper surface that is coplanar with an upper surface of an oxide layer, said dummy gate is located on a sacrificial oxide that is positioned atop a Si-containing substrate;

removing the dummy gate to provide a gate opening that exposes a portion of the sacrificial oxide, said gate opening defining a device channel in said Si-containing substrate;

removing the exposed portion of the sacrificial oxide in the gate opening;

forming a gate dielectric and amorphous Si gate in said gate opening;

implanting dopants in said amorphous Si gate and annealing the dopants in said amorphous Si gate to convert said amorphous Si gate into a polySi gate, while introducing localized strain to said device channel; and

removing the oxide layer and forming source/drain junctions in portions of the Si-containing substrate that adjoin the localized strained device channel.

2. The method of Claim 1 wherein said dummy gate has sidewalls that have an insulator spacer located thereon, said insulator spacer is positioned between said dummy gate and the oxide layer.

3. The method of Claim 1 wherein said removing of the dummy gate comprises chemical downstream etching or etching in KOH.

4. The method of Claim 1 wherein said removing the exposed portion of the sacrificial oxide comprises a chemical oxide removal (COR) step.

5. The method of Claim 4 wherein the COR step is carried out at a pressures of about 6 millitorr or less in a vapor or a plasma of HF and NH_3.

6. The method of Claim 1 wherein the device channel is doped by ion implantation and annealing prior to removing the exposed portion of the sacrificial oxide layer.

7. The method of Claim 1 wherein said forming said amorphous Si gate comprises deposition at a temperature of about 600°C or less and planarization.

8. The method of Claim 1 wherein the annealing is performed at a temperature of about 1000°C for a time period of greater than 5 seconds and in the presence of nitrogen.

9. The method of Claim 1 wherein the removing of the oxide layer comprises an etching process that is highly selective in removing oxide.

10. The method of Claim 1 wherein the source/drain junctions are formed by an angle implantation process and annealing.

11. The method of Claim 1 further comprising forming salicide regions on the source/drain junctions.

12. A MOSFET device comprising

a Si-containing substrate having a localized strained device channel and adjoining source/drain junctions;

a gate dielectric located on said localized strained device channel; and

a polySi gate located on said gate dielectric.

13. The MOSFET device of Claim 12 wherein the Si-containing substrate is an SOI substrate.

14. The MOSFET device of Claim 12 wherein the Si-containing substrate is a p-type Si-containing substrate.

15. The MOSFET device of Claim 12 wherein the gate dielectric is an insulator selected from the group consisting of SiO_2, Si_3N_4, SiON, $SiON_2$, perovskite-type oxides and combinations thereof.

16. The MOSFET device of Claim 12 wherein the polySi gate has sidewalls that have an insulator spacer located thereon.

17. The MOSFET device of Claim 12 further comprising salicide regions located on said source/drain junctions.

18. The MOSFET device of Claim 12 wherein the polySi gate is n- or p-type doped.

19. A MOSFET device comprising

a Si-containing substrate having a localized strained device channel and adjoining source/drain junctions having a depth of about 20 nm or less;

a gate dielectric located on said localized strained device channel; and

a polySi gate located on said gate dielectric.